Amendments to the Specification:

Please replace the paragraph bridging page 7 and page 8 with the following amended paragraph:

> In one implementation, each of processor switches PSW, memory switches MSW and switch crossbars SXB is fabricated as a separate semiconductor chip. In one implementation, each processor switch PSW is fabricated as a single semiconductor ship, each switch crossbar SXB is fabricated as two or more semiconductor chips that operate in parallel, each memory crossbar MXB is fabricated as two or more semiconductor chips that operate in parallel, and each memory track T is fabricated as a single semiconductor chip. One advantage of each of these implementations is that the number of off-chop interconnects is minimized. Such implementations are disclosed in two copending patent applications entitled "SLICED CROSSBAR ARCHITECTURE WITH INTER-SLICE COMMUNICATION," now U.S. Pat. No. 6,970,454~~serial number (TBS), filed (TBS), attorney docket number 16(BLV005001)~~ and "SLICED CROSSBAR ARCHITECTURE WITH NO INTER-SLICE COMMUNICATION," now U.S. Pat. No. 6,961,803~~serial number (TBS), filed (TBS), attorney docket number 19(BLV004001)~~